20.4 A Highly Linear Direct-Conversion Transmit Mixer Transconductance Stage with Local Oscillation Feedthrough and I/Q Imbalance Cancellation Scheme

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Demand for higher data rate in WLAN systems is driving the performance requirements of the radio front-end ever higher [1]. Some of the requirements of the next generation WLAN transmitters are low transmit EVM, a low local oscillator feed-through (LOFT), a small I/Q imbalance, a wide gain-control range, and preferably a minimum number of real-time calibrations. In this paper, a highly linear transmit mixer transconductance stage is presented that incorporates a wide gain-control range and a *one-time* LOFT and I/Q imbalance cancellation scheme to meet these goals.

Figure 20.4.1 shows a simplified block diagram of a direct-conversion transmitter along with an envelope detector and circuitry to amplify the detected envelope. For sinusoidal I/Q inputs at BB_I and BB_Q, the high-frequency envelope detector generates a filtered and amplified baseband ripple with spectral components at F_{BB} due to LOFT and at $2\times F_{BB}$ due to I/Q imbalance (Fig. 20.4.3).

The core of the transconductance stage is shown in Fig. 20.4.2 [2]. The input pair, M1 and M2, is put in feedback to linearize the effective transconductance. The signal currents flow through M3 and M4 and are mirrored to M5 and M6. The effective transconductance of the circuit is 1/R1×R9/R7 under high levels of degeneration. R3 to R12 are the degeneration resistors used to reduce the device offsets. Note that R1 and R2 are not used as part of gain control. When R1 and R2 are changed, the overall ratio of the signal to offsets will change since the offset contribution of all the devices in the signal path following R1 and R2 will remain constant whereas all offsets prior to R1 and R2 will scale by the change in the gain. The circled devices in Fig. 20.4.2 constitute the proposed gain-control scheme. The gates of both the shunt device, M7, and the cascode devices, M5 and M6, are tied together. To the first order, the current gain will be given by the ratio of their W/L's. Therefore, the gain-control scheme is independent of process, voltage, and temperature variation and possesses a high linearity [3]. A variable gain is implemented by using multiple shunt devices.

Two types of LOFT exist in a direct-conversion up-converter mixer. The first type, baseband LOFT (BB_LOFT), originates from the device offsets in the DAC, LPF, and the transconductance stage. The offsets will up-convert and generate a LOFT component at the output of the mixer. The second type, RF_LOFT, is a direct-coupling component either through parasitic capacitance or mutual inductance. The two types of offsets require a dual cancellation scheme to cancel both components at their sources. Shown in Fig. 20.4.2 are the two sets of currents that remove LOFT by introducing an artificial offset. First, BB_LOFT_IP and BB_LOFT_IN cancel all the offsets prior to the gain-control stage. The baseband gain control is also done at these nodes and will scale the cancellation current by the same factor, maintaining proper cancellation current without the need for a re-calibration. Note that the devices M5 and M6 are after the gain-control shunt devices and could contribute a BB_LOFT at very high attenuation settings. In practice, these devices can be made sufficiently large to have minimal offsets. A second set of correction currents, RF_LOFT_IP and RF_LOFT_IN, are at the drain nodes of M5 and M6. The injection is done immediately before the switching quads of the mixer but after the gain-control shunt devices so that the cancellation currents will not be affected by the gain change. Each set of correction currents are binary weighted current DACs (IDACs).

A straight-forward algorithm can be devised to separate the two LOFT components and remove LOFT as well as I/Q imbalance. Figure 20.4.3 shows a flow chart of the proposed algorithm. First, a set of I and Q sinusoids is injected at baseband. Spectral analysis of the detector's output reveals the magnitude of the LOFT (F_{LO}) and I/Q imbalance (F_{IM}) [4]. Second, the gain is set to minimum to significantly attenuate the baseband offsets. The remaining LOFT is from RF. Third, the RF_LOFT is cancelled using the RF IDAC. Fourth, with the RF_LOFT cancelled, the gain is changed to maximum. This will allow a good visibility in the event that the BB_LOFT is small. Fifth, the remaining BB_LOFT can be cancelled using the BB IDAC. Note that the maximum amount of LOFT suppression will depend on the resolution of both IDACs and the achievable amount of suppression of the BB_LOFT in Step 2. Lastly, keeping the gain at maximum, $2\times F_{BB}$ components can be removed by adjusting the baseband signal's phase and amplitude to correct the I/Q imbalance. The phase and amplitude information can then be used to pre-distort the modulated signal in the DSP.

The chip is fabricated in a 0.18μm CMOS process and is in use in a multi-band WLAN transceiver. Figure 20.4.4 shows the two-tone test result of the transmitter. To allow maximum visibility into the linearity of the transconductance stage, the transconductance stage is set to minimum gain and the following RF drivers are set to maximum gain. The two-tone inputs, running at the maximum swing level of the DAC ($1V_{pp}$) at 5 and 6MHz, generates 3rd-order intermodulation components that are more than 52dBc down from the signal tones.

Figure 20.4.5 shows the plots of transmitter output before and after the proposed calibration at maximum and minimum gain settings. Gain steps are 2.5dB with a 17.5dB of range. I/Q CW tones are applied at 1MHz with the LO running at 5.24GHz. The post calibration LOFT is better than 32dBc and image rejection is better than 46dBc for all gain settings. The transmitter as a whole is capable of producing an output EVM of <–40dB in the A band (Fig. 20.4.6) and <-41dB in the G band.

A highly linear transconductance stage is presented that incorporates gain-independent cancellation of LOFT and I/Q imbalance. The achievable performance of the scheme is limited to the resolution of the IDACs and the amount of calibration time available at the start-up of the circuit. Results indicate that no other calibration other than at startup is necessary to maintain sufficient performance. The chip micrograph is shown in Fig. 20.4.7.

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[2] I. Mehr et al., "A CMOS Continuous-Time G_m-C Filter for PRML Read Channel Applications at 150 Mb/s and Beyond," *IEEE J. Solid-State Circuits*, vol. 32, no. 4, pp. 499-513, April, 1997.
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[4] J. Cavers, "New Methods for Adaptation of Quadrature Modulators and Demodulators in Amplifier Linearization Circuits," *IEEE Trans. Vehicular Technology*, vol. 46, no. 3, pp. 707-716, Aug., 1997.

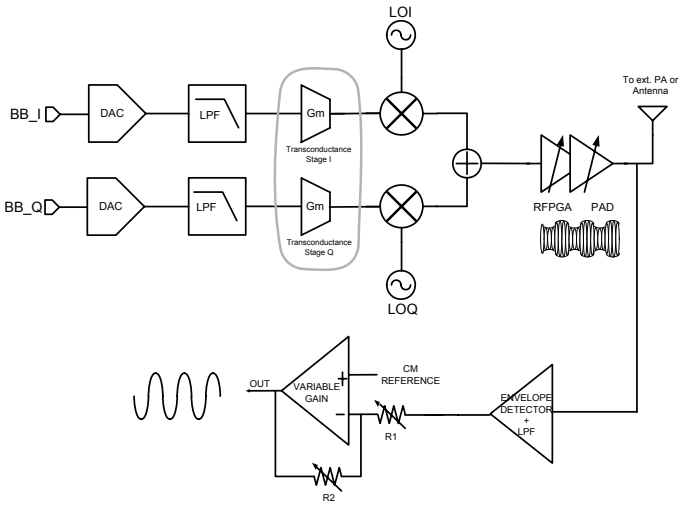

Figure 20.4.1: Transmitter architecture.

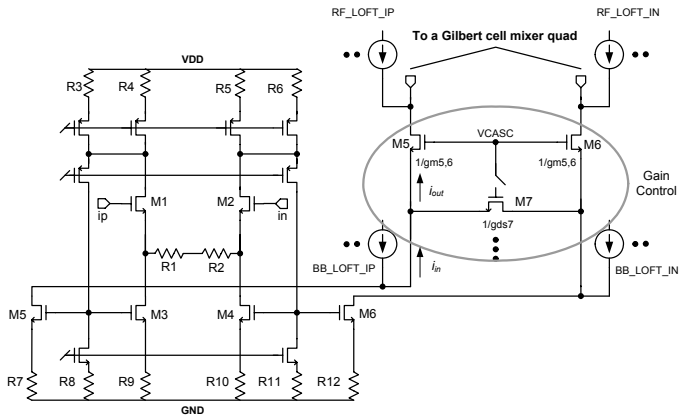

Figure 20.4.2: Transconductance-stage schematic.

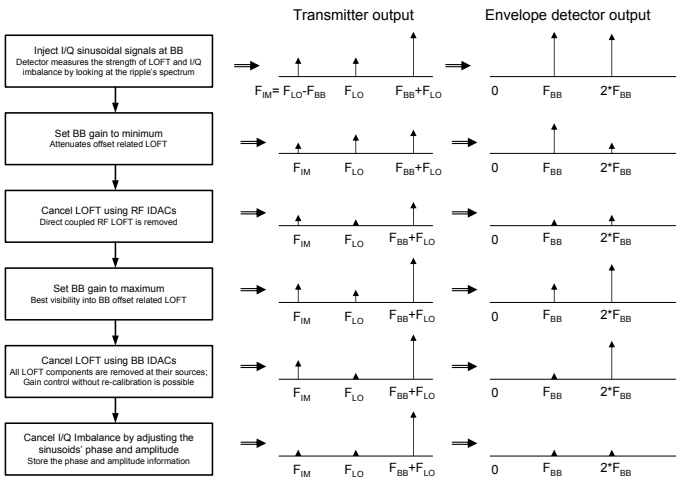

Figure 20.4.3: LOFT/IQ calibration algorithm.

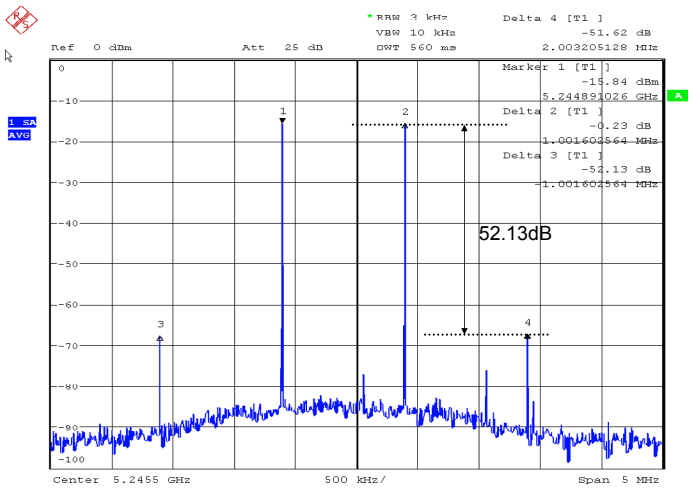

Figure 20.4.4: TX two-tone linearity test.

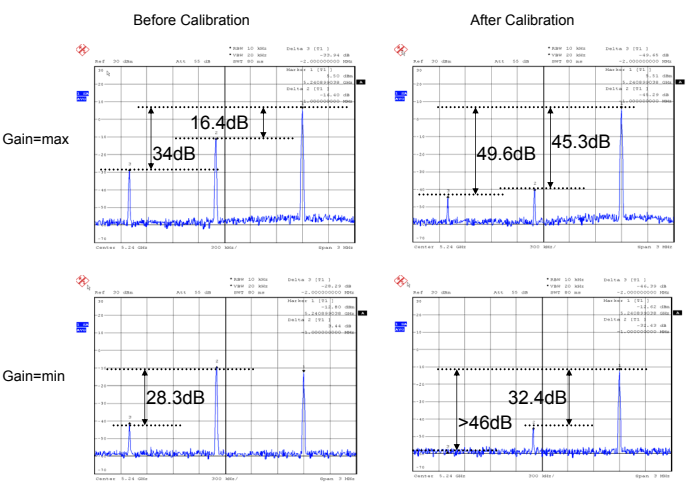

Figure 20.4.5: TX output before and after calibration.

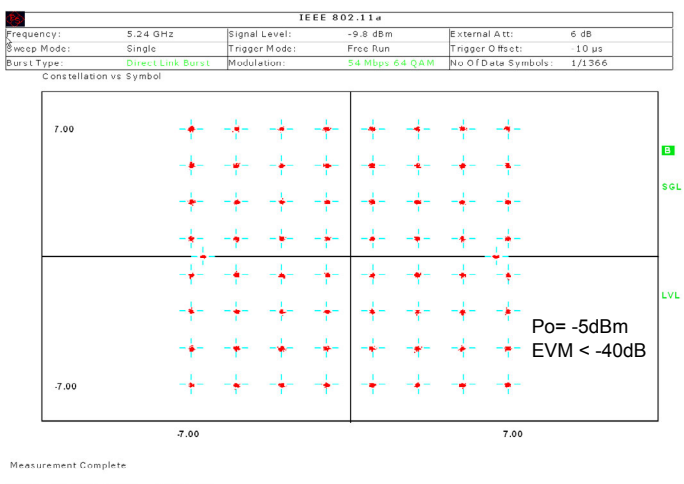

Figure 20.4.6: Constellation diagram of the entire TX chain output at 5.24GHz after calibration.

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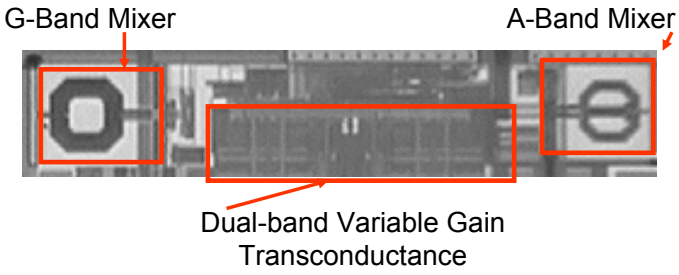

Figure 20.4.7: Chip Micrograph.

